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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): RAJAGOPALAN, Sarathy *et al.*

Serial No.: 09/465,131

Filed: December 16, 1999

For: METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

Art Unit: 2859

Examiner: Guadalupe, Yaritza

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, U.S. Patent and Trademark Office, on the date below.

March 3 2003 Rhonda L. Mason
Date Rhonda L. Mason

SUPPLEMENTAL APPEAL BRIEF UNDER 37 C.F.R. § 1.193(b)(2)

Box Appeals
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Appellant hereby requests reinstatement of the appeal of the final rejection of Claims 1-6 in the subject application and submits this supplemental appeal brief under 37 C.F.R. § 1.193(b)(2) in response to the Office Action mailed on December 09, 2002 (Paper No. 15).

(1) Real Party in Interest

The real party in interest in the subject application is LSI Logic Corporation.

(2) Related Appeals and Interferences

No related appeals or interferences are known to appellant.

(3) Status of Claims

Claims 1-6 are pending in the subject application.

Claims 1, 4 and 5 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (APA) in view of U.S. Patent 5,997,174 to Wyland (*Wyland*).

Claims 2 and 3 stand finally rejected under 35 USC §103(a) as being unpatentable over admitted prior art in view of *Wyland* as applied to Claims 1, 4 and 5 and further in view of U.S. Patent No. 6,131,579 to Thorson et al. (*Thorson*).

Claim 6 stands finally rejected under 35 USC §103(a) as being unpatentable over admitted prior art in view of *Wyland* and further in view of U.S. Patent No. 5,585,577 to Lemoine (*Lemoine*).

(4) Status of Amendments

The amendments filed on May 8, 2001 (Amendment "A"), September 6, 2001 (Amendment "B"), October 24, 2001 (Amendment "C"), and May 1, 2002 (Amendment "D") have been entered.

(5) Summary of Invention

The present invention provides a thermal profiling device for accurately measuring the temperature at the interface between a semiconductor die and a packaging substrate of an integrated circuit during a reflow process in which the die is attached to the substrate. In one aspect of the present invention, a thermal profiling device for a flip-chip integrated circuit includes a packaging substrate of a flip-chip integrated circuit; a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured to an upper surface of the packaging substrate; and a thermocouple secured directly to the active circuit surface of the semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.

(6) Issues on Appeal

The following issues are on appeal:

Issue 1: Whether motivation exists in the cited prior art for modifying *Wyland* to arrive at the claimed invention; and

Issue 2: Whether the modification proposed by the rejection arrives at the claimed invention.

(7) Grouping of Claims

A statement that the claims of a group do not stand

or fall together is not included with this supplemental appeal brief.

(8) Argument

No motivation exists in the cited prior art for modifying *Wyland* to arrive at the claimed invention

Claim 1 recites a thermocouple secured directly to the active circuit surface of a semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process. The rejection admits that APA does not disclose the thermocouple secured directly to the active circuit surface of the semiconductor die as recited in Claim 1. The rejection argues that *Wyland* discloses locating a thermocouple (117) secured on a junction between surfaces (113, 114) for measuring and controlling a junction/interface temperature and that it would be obvious to provide a thermocouple secured to the semiconductor die for measuring the junction/interface temperature as taught by *Wyland* to provide an enhancement for measuring die interface temperature. Appellant traverses the rejection as follows.

As *Wyland* explains in the abstract and in column 4, lines 47 *et seq.*, the thermocouple (117) is used to determine the junction temperature of the semiconductor die (122) inside a component package (121) by measuring the thermal resistivity of a board or coupon (113) on which the package (121) is mounted.

The rejection errs in alleging that *Wyland* discloses locating a thermocouple (117) secured on a "junction" between surfaces (113, 114) for measuring and controlling a "junction/interface" temperature. The rejection apparently

confuses the junction of the semiconductor die (122) inside the package (121) referred to in *Wyland* and the interface between the surfaces (113, 114) adjoining the thermocouple (117) by the device of combining the two terms "junction" and "interface" with a slash to imply that they are equivalent. As may clearly be seen from FIG. 1A in *Wyland*, the junction of the semiconductor die (122) is inside the package (121), while the interface between the surfaces (113, 114) is outside the package (121). Because the junction of the semiconductor die is inside the package (121) and the interface between surfaces (113,114) is outside the package (121), they are not equivalent as implied by the rejection. Because the junction of the semiconductor die and the interface between surfaces (113,114) are not equivalent, the rejection fails to establish a nexus between the semiconductor junction in *Wyland* and the claimed subject matter of a thermocouple secured between the active circuit surface of a die and an upper surface of a package substrate.

The rejection further errs in failing to consider the claim limitation of measuring a temperature of the active circuit surface of the semiconductor die during a reflow process in determining patentability of Claims 1-6 under 35 U.S.C. § 103(a) as explained at MPEP § 2143.03 (2100-126):

> "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). 'All words in a claim must be considered in judging the patentability of that claim against the prior art.' *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)."

Specifically, *Wyland* is directed to determining the temperature of a junction in a semiconductor die (see column 1, lines 10-12), which changes more slowly over time and over a smaller temperature range as compared to the temperature of the active circuit surface of a semiconductor die during a reflow process. Because the temperature changes are much more rapid during a reflow process in which the die is attached to the substrate than in the operation of an integrated circuit, the location of the thermocouple is much more critical to the accuracy of the temperature measurements in a reflow process than in applications that monitor slower and smaller variations in temperature, such as the junction temperature of an integrated circuit die disclosed in *Wyland*. Because the location of the thermocouple is less critical in *Wyland* than in the claimed reflow process, *Wyland* would realize no apparent benefit from the modification proposed by the rejection. Because *Wyland* would realize no apparent benefit from the modification proposed by the rejection, there is no motivation in *Wyland* to make the proposed modification as required by MPEP § 2143.01 (2100-124).

Further, the rejection fails to show that the proposed modification would be of any benefit to the intended purpose of *Wyland*. *Wyland* is not directed to measuring the temperature of the active circuit surface of a semiconductor die during a reflow process, and the rejection fails to provide a convincing line of reasoning to show that the proposed modification to *Wyland* would in fact enhance the determination of the junction temperature of the semiconductor die (122) as disclosed in *Wyland*. Because there is no apparent benefit to *Wyland* to make the proposed modification, there is no motivation in the reference to make the proposed modification as required by MPEP § 2143.01 (2100-124).

Still further, subjecting the package (121) containing the semiconductor die (122) in *Wyland* to the temperatures encountered in a reflow process described in the specification on page 1, lines 1 *et seq.* and recited in Claim 1 would likely damage or destroy a typical integrated circuit package such as exemplified by package (121), thereby rendering *Wyland* unsuitable for its intended purpose. Because the proposed modification would render *Wyland* unsuitable for its intended purpose, there is no motivation in the reference to make the proposed modification as required by MPEP § 2143.01 (2100-124).

The modification proposed by the rejection fails to arrive at the claimed invention

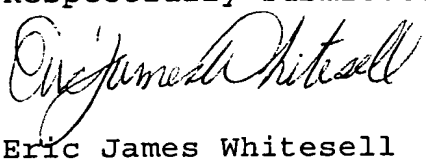
Because the rejection errs in failing to consider the claim limitation of measuring a temperature of the active circuit surface of the semiconductor die during a reflow process as recited in Claim 1, the proposed modification fails to arrive at the claimed invention as a whole. Further, the junction inside the semiconductor die taught in *Wyland* is not equivalent to the active circuit surface of the die as recited in Claim 1. Because the proposed modification fails to arrive at the claimed invention, Claims 1 and 6 are not obvious over *Wyland* under 35 U.S.C. § 103.

Conclusion

In summary, the rejection of Claims 1-6 is based upon a proposed modification for which no motivation exists in *Wyland*, which would render *Wyland* unsuitable for its intended purpose, and which does not arrive at the claimed invention as a whole. Because no reasonable motivation has been

established for making the proposed modification, and because the proposed modification does not arrive at the claimed invention, Claims 1 and 6 are non-obvious under 35 U.S.C. § 103 over *Wyland*. Because the rejections of Claims 2-5 rely on the same errors made in the rejection of Claims 1 and 6, Claims 2-5 are likewise non-obvious under 35 U.S.C. § 103.

Respectfully submitted,



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APPENDIX

Claims

1. A thermal profiling device for a flip-chip integrated circuit comprising:

a packaging substrate of a flip-chip integrated circuit;

a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured to an upper surface of the packaging substrate; and

a thermocouple secured directly to the active circuit surface of the semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.

2. The thermal profiling device of Claim 1 wherein the thermocouple is secured using an adhesive.

3. The thermal profiling device of Claim 2 wherein the adhesive comprises an epoxy.

4. The thermal profiling device of Claim 1 wherein the active circuit surface has electrically conductive bumps formed thereon and the upper surface of the packaging substrate includes a plurality of bonding pads wherein the semiconductor die is positioned on the packaging substrate such that the electrically conductive bumps are in electrical contact with the plurality of bonding pads.

5. The thermal profiling device of Claim 4 wherein the packaging substrate and the semiconductor die are secured

in place by a solder bond between the electrically conductive bumps and the plurality of bonding pads.

6. A thermal profiling device for a flip-chip integrated circuit comprising:

a packaging substrate of a flip-chip integrated circuit having a first surface and a second opposite surface;

an opening passing through the second opposite surface and through the first surface of the packaging substrate;

a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured to the first surface of the packaging substrate; and

a thermocouple secured directly to the active circuit surface of the semiconductor die through the opening for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.